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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,197	06/24/2004	Takashi Mita	30391-17	9239

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EXAMINER	
FENNEMA, ROBERT E	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/500,197	MITA ET AL.	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 have been considered. Claims 1 and 11 amended as per Applicant's request. Claims 21-22 added as per Applicants request.

Claim Objections

2. Claim 22 is objected to in Line 5, it is believed that "form" should read "from", and has been treated as such for the remainder of the Office Action, however, appropriate correction or clarification is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 4, 6-7, 9-10, 11, 14, 16-17, and 19-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Trimberger et al. (USPN 5,646,545, herein Trimberger).

5. As per Claim 1, Trimberger teaches: A logic computing system comprising:

a plurality of data storage units which store a plurality of configuration data modules (Abstract, the programmed CLB's) to be retrieved from outside the logic computing system (Column 17, Lines 38-47, the FPGA receives its programming off-

chip), wherein each of the configuration data modules includes a look up table (Column 6, Lines 59-62); and

a logic computing unit (Abstract, the PLD) which includes a plurality of programmable logic circuits (Abstract, the programmable logic elements configure the CLB's and the interconnects),

wherein said logic computing unit provides a logical function value of logic input data as logic output data, by referring to at least one configuration data module retrieved and stored in at least one of said plurality of data storage units (See Figures 3 or 11. Also see Column 1, Lines 18-20) while another of said plurality of configuration data modules is being retrieved from outside the logic computing unit and stored in another one of said data storage units (Column 17, Lines 38-47, the FPGA receives its programming off-chip, while the FPGA is still active).

6. As per Claim 11, Trimberger teaches: A logic computing method comprising:

retrieving at least one of a plurality of configuration data modules, each of which includes a look up table (Column 6, Lines 59-62), from outside a logic computing system (Column 17, Lines 38-47, the FPGA receives its programming off-chip);

storing the retrieved at least one of the plurality of configuration data modules in a corresponding at least one of a plurality of data storage units inside the logic computing system (Abstract, the programmed CLB's);

preparing a logic computing unit (Abstract, the PLD) inside the logic computing system, wherein the logic computing unit includes a plurality of programmable logic

circuits (Abstract, the programmable logic elements configure the CLB's and the interconnects);

referring by said logic computing unit to at least one configuration data module stored in at least one of the plurality of data storage units (Column 1, Lines 14-20); and

providing a logical function value of logic input data as logic output data, based on the configuration data module referred to by said logic computing unit (See Figures 3 or 11. Also see Column 1, Lines 18-20), while retrieving another of said plurality of configuration data modules from outside the logic computing unit and storing it in another one of said data storage units (Column 17, Lines 38-47, the FPGA receives its programming off-chip, while the FPGA is still active).

7. As per Claim 4, Trimberger teaches: The logic computing system according to claim 1, comprising a selector which selects at least one of said plurality of data storage units,

wherein said logic computing unit refers to the configuration data module which is stored in said data storage unit selected by said selector (Column 1, Lines 15-17).

Claim 14 is substantially similar to Claim 4 and is rejected for the same reasons.

8. As per Claim 6, Trimberger teaches: The logic computing system according to claim 1, comprising:

a parameter register which stores all or part of internal parameters of said logic computing unit for stacking (Column 2, Lines 22-23 and Column 7, Lines 23-26);

a detector which detects a call and a call back by one of the plurality of configuration data modules to another one of the plurality of configuration data modules (Column 26, Line 60 – Column 27, Line 14, a detector would be required to make the call/call back); and

a controller which controls logic computing by said logic computing unit,

wherein said controller:

stores the internal parameters of said logic computing unit in said parameter register, when said detector detects a call by one of the plurality of configuration data modules to another one of the plurality of configuration data modules as a subroutine (Column 7, Lines 23-26, as the configuration changes due to a call/return, the parameters are clocked into the register, and a controller must be present to direct the register to do this); and

restores the internal parameters stored in said parameter register in said logic computing unit, when said detector detects a call back to one of the plurality of configuration data modules (Column 7, Lines 26-50, also see Column 22, Lines 11-14).

Claim 16 is substantially similar to Claim 6 and is rejected for the same reasons.

9. As per Claim 7, Trimberger teaches: The logic computing system according to claim 1, further comprising a loader which loads the configuration data module(s) to one or more of said plurality of data storage units (Column 6, Lines 53-55, to be reconfigured a loader is required),

wherein each of said plurality of data storage units stores the configuration data module rewritably (Column 6, Lines 51-52).

Claim 17 is substantially similar to Claim 7 and is rejected for the same reasons.

10. As per Claim 9, Trimberger teaches: The logic computing system according to claim 1, comprising:

a parameter buffer which stores all or part of internal parameters of said logic computing unit for handing (Column 2, Lines 22-23 and Column 7, Lines 23-26);

a detector which detects a call or a call back by one of the plurality of configuration data modules to another one of the plurality of configuration data modules (Column 26, Line 60 – Column 27, Line 14, a detector would be required to make the call); and

a controller which controls logic computing by said logic computing unit, wherein said controller:

stores the internal parameters of said logic computing unit in said parameter buffer, when said detector detects a call or a call back by one of the plurality of configuration data modules to another one of the plurality of configuration data modules (Column 7, Lines 23-26, as the configuration changes due to a call/return, the parameters are clocked into the register, and a controller must be present to direct the register to do this); and

inputs the parameters stored in said parameter buffer to said logic computing unit, when the configuration data module which is called or called back is arranged so

that it can be referred to by said logic computing unit (Column 7, Lines 26-50, which discusses how the saved register values can be routed to be used by any configuration that wishes to use it).

Claim 19 is substantially similar to Claim 9 and is rejected for the same reasons.

11. As per Claim 10, Trimberger teaches: The logic computing system according to claim 1, comprising a compiler which creates each of the plurality of configuration data modules based on each of a plurality of source program modules (Examiner is taking official notice that some kind of compiler is required to program an FPGA (or any other kind of programmable logic hardware) or run any kind of source program on a computer). Claim 20 has substantially similar limitations to Claim 10 and is rejected for the same reasons.

12. As per Claim 21, Trimberger teaches: The logic computing system according to claim 1, further comprising

a loader which loads the configuration data module(s) from outside the logic computing unit to one or more of said plurality of data storage units(Column 17, Lines 31-33), where:

said logic computing unit generates a load command in the process of computing by said plurality of programmable logic circuits (Column 17, Lines 52-55); and

said loader loads the configuration data module which is indicated by the load command in the process (Column 17, Lines 31-33 and 52-58, the loader loads configuration data, and the FPGA initiates reconfiguration of CLB's as necessary).

13. As per Claim 22, Trimberger teaches: The logic computing method according to claim 11, further comprising:

generating a load command in the process of computing by said plurality of programmable logic circuits (Column 17, Lines 52-55); and

loading by a loader the configuration data module which is indicated by the load command in the process from outside the logic computing unit to one of said plurality of data storage units (Column 17, Lines 31-33 and 52-58, the loader loads configuration data, and the FPGA initiates reconfiguration of CLB's as necessary).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 2 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Trimberger, in view of Butts et al. (USPN 5,036,473, herein Butts).

16. As per Claim 2, Trimberger teaches: The logic computing system according to claim 1, but fails to teach wherein:

said plurality of data storage units form a shift register; and

said logic computing unit refers to the configuration data module(s) stored in one or more of said plurality of data storage units included in said shift register.

While Trimberger teaches an array of CLB's, which hold configurable data modules, which can be configured and programmed (Column 1, Line 19), he does not explicitly teach how this programming is accomplished, or what the structure of these CLB's are. Butts teaches that in at least one common CLB configuration which is well known in the art, reconfigurable features are controlled by bits in a shift register, and the configuration is shifted into the array of CLB's. Therefore, the way that CLB's are designed to be programmed requires them to function as shift registers. Given the need to have a method to program the reconfigurable logic in Trimberger's invention, and with Butts providing one, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Butt's programming teachings with Trimberger's system, which would have the effect of having the CLB's act as shift registers.

Claim 12 has substantially similar limitations to this claim and has been rejected for the same reasons.

17. Claims 3 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Trimberger and Butts, further in view of Liu et al. (herein Liu).

18. As per Claim 3, Trimberger and Butts teaches: The logic computing system according to claim 2, but fails to teach:

wherein said shift register shifts the configuration data modules among said plurality of data storage units circularly.

Trimberger and Butts have taught that the data storage units containing configuration data modules (the programmed CLB) are arranged as shift registers as shown in the previous claims, but have not taught that the shift registers are arranged in a circular fashion. However, Liu teaches a method for partitioning a system similar to Trimberger's, which also offers an advantage of outperforming the force-directed scheduling method (Abstract) used by Trimberger (Trimberger, Column 30, Lines 19-23). As can be seen by Figure 1, the configurable logic is laid out as a circular shift register. Given the advantage of increased performance over the scheduling method employed by Trimberger, one of ordinary skill in the art at the time the invention was made would have made use of Liu's invention, which would have also made the shift registers need to be laid out in a circular fashion.

Claim 13 is substantially similar to claim 3 and is rejected for the same reasons.

19. Claims 5 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Trimberger, in view of Liu.

20. As per Claim 5, Trimberger teaches: The logic computing system according to claim 4, but fails to teach:

wherein said selector selects one of said plurality of data storage units from among said plurality of data storage units circularly.

Trimberger has taught a selector which selects at least one of the data storage units through an interconnect system, but does not teach that the data is selected circularly. However, Liu teaches a method for partitioning a system similar to Trimberger's, which also offers an advantage of outperforming the force-directed scheduling method (Abstract) used by Trimberger (Trimberger, Column 30, Lines 19-23). As can be seen by Figure 1, the configurable logic is laid out in a circular fashion. Given the advantage of increased performance over the scheduling method employed by Trimberger, one of ordinary skill in the art at the time the invention was made would have made use of Liu's invention, which would have also made the shift registers need to be laid out in a circular fashion.

Claim 15 is substantially similar to claim 5 and is rejected for the same reasons.

21. Claims 8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Trimberger, in view of Patterson et al. (herein Patterson).

22. As per Claim 8, Trimberger teaches: The logic computing system according to claim 7, comprising:

a detector which detects a call by one of the plurality of configuration data modules to another one of the plurality of configuration data modules (Column 26, Line 60 – Column 27, Line 14, a detector would be required to make the call); and

a controller which controls logic computing by said logic computing unit, wherein said controller (Column 7, Lines 23-26):

said loader loads the configuration data module as the subroutine which is indicated by the load command to one of said plurality of data storage units (Column 6, Lines 53-55, to be reconfigured a loader is required), but fails to teach:

searches, when said detector detects a call by one of the plurality of configuration data modules to another one of the plurality of configuration data modules as a subroutine, said plurality of data storage units for the configuration data module as the subroutine; and

sends a load command to said loader, in a case where the configuration data module as the subroutine is not searched out.

Trimberger has taught a detector which can detect calls, and a controller to tell a loader to load modules, but has not taught searching the plurality of data storage units for a configurable data module as specified by a call, and then loading that module if it was not found in a search. Trimberger teaches these things to account for the fact that there are not enough configurable logic elements in his system to handle the entire program, so it is broken up and partitioned into pieces, which can be swapped in and out. Patterson has taught a method called paging which is used to allow a very large program (or programs), much bigger than main memory, to be used by a computer, by

swapping pages in and out of memory as they are required, creating the illusion of a much larger memory space (Pages 439-441). Foldoc further describes paging and page faults, and is referred to as extrinsic evidence on the functionality of paging (see "paging" and "page fault" documents). The advantage of paging, as stated earlier, is virtually increasing the amount of memory that appears to be available in a system by swapping "pages" of memory in and out of main memory, in a very similar way to how Trimberger swaps configuration modules in and out of the CLB's. The difference is that in paging, a search is first conducted among the pages in memory, and the appropriate page is then loaded if not found (see "page fault" entry of Foldoc), which has the further obvious advantage of not having to reconfigure/fetch on every call. Given these advantages, it would have been obvious to one of ordinary skill in the art at the time the invention was made to fully incorporate the idea of paging into Trimberger's invention by searching for configurations before fully reloading the data storage units to maximize performance.

Claim 18 is substantially similar to claim 8 and is rejected for the same reasons.

Response to Arguments

23. Applicant's arguments filed 1/26/2007 have been fully considered but they are not persuasive. Applicant has made arguments that essentially boil down to Trimberger (and the other references in the case of 103 rejections) not teaching the newly added subject material, namely, retrieving configuration data modules from outside the logic system, and retrieving these modules while the system is active (an input generating an

output). However, Trimberger teaches both of these limitations in Column 17. Lines 37-41 show that the data comes from off-chip (this could be considered inherent, as something must configure the FPGA), and Lines 46-47 clearly state that the FPGA is active during reconfiguration. Applicant has pointed to one programming embodiment which states that the chip is idle until a signal arrives, however, in Column 18, Lines 23-27, a second embodiment is disclosed in which the chip does not sit idle waiting for a signal. Given that Trimberger clearly states that the FPGA can be reprogrammed from off-chip while active, Examiner asserts that Trimberger teaches the new claim limitations. Applicant has made arguments asserting that Trimberger has slower performance than the current invention due to the implementation, however these differences are immaterial, as they are not represented in the claim language.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:45-6:15.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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